

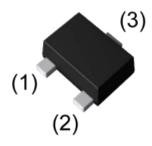
SSCU180N20GS9

N-Channel Enhancement Mode MOSFET with ESD Protection

> Features

V _{DS}	V _{GS}	R _{DS(ON)} Typ.	ID
		180mΩ@4V5	
20V	\pm 12V	230mΩ@2V5	1.2A
		330mΩ@1V8	

Pin configuration



<u>SOT-723</u>

> Description

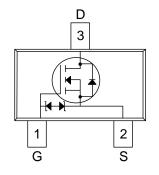
This device is a N-Channel enhancement mode MOSFET, which is produced with high cell density and DMOS trench technology. This device particularly suits low voltage applications, especially for battery powered circuits, the tiny and thin outline saves PCB consumption.

this device has ESD protection structure.

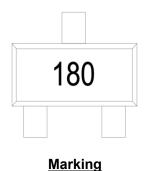
- > Applications
- Replace Digital Transistor
- Battery Operated Systems
- Power Supply Converter Circuits
- Load/Power Switching cell Phones

> Ordering Information

Device	Package	Shipping
SSCU180N20GS9	SOT-723	8000/Reel



Pin Configuration (Top View)





> Absolute Maximum Ratings ($T_A=25^{\circ}C$ unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V _{DSS}	Drain-to-Source Voltage	20	V
V _{GSS}	Gate-to-Source Voltage	±12	V
١D	Continuous Drain Current ^a	1.2	А
I _{DM}	Pulsed Drain Current ^b	4.8	A
PD	Power Dissipation °	0.3	W
TJ	Operation junction temperature	-55~150	°C
Тѕтс	Storage temperature range	-55~150	°C

> Thermal Resistance Ratings (T_A=25 $^{\circ}$ C unless otherwise noted)

Symbol	Parameter	Typical	Maximum	Unit
Reja	Junction-to-Ambient Thermal Resistance ^a	320	416	°C/W

Note:

- a. The value of R_{θJA} is measured with the device mounted on 1 in² FR-4 board with 2oz.copper, in a still air environment with T_A=25 °C. The value in any given application depends on the user is specific board design. The power dissipation is based on the t≤10s thermal resistance rating.
- b. Repetitive rating, pulse width limited by junction temperature.
- c. The power dissipation P_D is based on $T_{J(MAX)}$ =150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.



SSCU180N20GS9

> Electrical Characteristics ($T_A=25^{\circ}C$ unless otherwise noted)

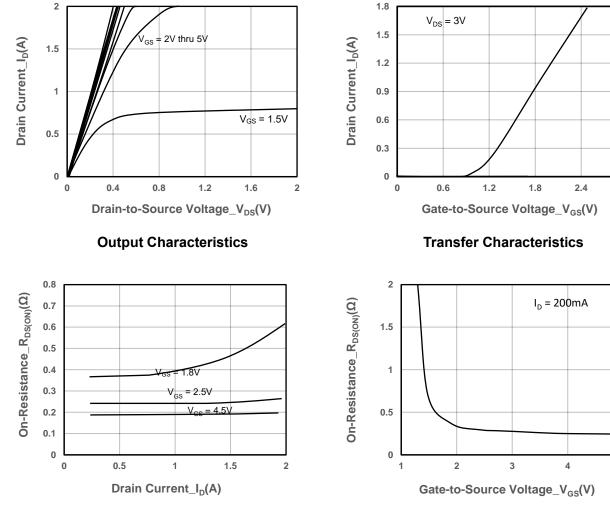
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250uA	20			V
Gate Threshold Voltage	V _{GS(th)}	V_{DS} = V_{GS} , I_D = 250uA	0.35	0.6	1	V
		V _{GS} = 4.5V, I _D = 0.6A		180	450	
Drain-Source On-Resistance	R _{DS(on)}	V _{GS} = 2.5V, I _D = 0.5A		230	765	mΩ
		V _{GS} = 1.8V, I _D = 0.35A		330	1300	
Zero Gate Voltage Drain Current	IDSS	V _{DS} = 16V, V _{GS} = 0V			1	μA
Gate-Source Leak Current	Igss	$V_{GS} = \pm 12V, V_{DS} = 0V$			±10	μA
Transconductance	G _{FS}	V _{DS} = 5V, I _D = 0.5A		11		s
Forward Voltage	V _{SD}	V _{GS} = 0V, I _S = 0.15A		0.7	1.3	V
Input Capacitance	Ciss			53		
Output Capacitance	Coss	$V_{DS} = 16V, V_{GS} = 0V,$		15		pF
Reverse Transfer Capacitance	C _{RSS}	f = 200KHz		12		
Turn-on Delay Time	T _{D(ON)}			6.2		
Rise Time	Tr	V _{GS} =4.5V, V _{DS} = 10V,		4.9		
Turn-off Delay Time	T _{D(OFF)}	I _D = 0.5A		18.5		ns
Fall Time	T _f			7.7		
Total Gate Charge	Q_{G}			1.2		
Gate to Source Charge	Q _{GS}	$V_{GS} = 10V, V_{DS} = 15V$		0.16		nC
Gate to Drain Charge	Q_{GD}	I _D = 0.2A		0.15		



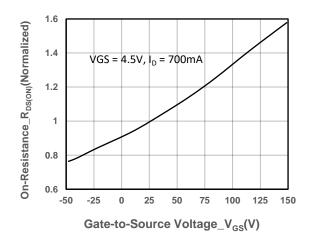
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> Typical Performance Characteristics ($T_A=25^{\circ}C$ unless otherwise noted)

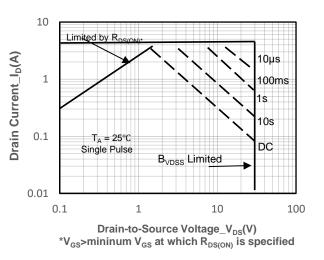


On-Resistance vs. Drain Current and Gate Voltag



On-Resistance vs. Junction Temperature

On-Resistance vs. Gate-to-Source Voltage

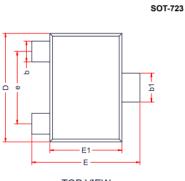


Safe Operating Area vs. Junction-to-Ambient

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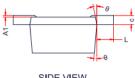


Package Information \triangleright



TOP VIEW

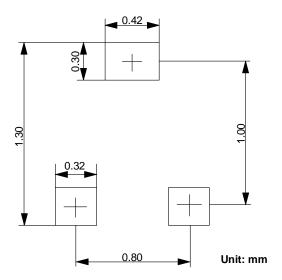
SIDE VIEW



SIDE VIEW

DIM		Millimeters				
	Min.	Тур.	Max.			
Α	0.43	-	0.55			
A1	0.00	-	0.05			
b1	0.27		0.37			
b	0.17	-	0.27			
С	0.08	0.13	0.18			
D	1.15	1.20	1.25			
Е	1.15	1.20	1.25			
E1	0.75	0.8	0.85			
е	0.80Ref.					
L	0.15	0.2	0.25			
θ	7°Ref.					

Suggested Pad Layout \succ





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